Listing of Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Claim 1 (Withdrawn): A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate; forming a diffusion region in said substrate adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region;

said step of forming said self-aligned opening comprising the steps of: forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film;

forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

removing said first insulation film exposed at a bottom of said contact hole selectively with respect to said diffusion region;

wherein said step of forming said first insulation film is conducted by a plasma CVD process, with a high-frequency power set smaller than a high-frequency power in which said first insulation film contains H_2O with an amount of about 2.4 wt %.

Claim 2 (Withdrawn): A method as claimed in claim 1, wherein said high-frequency power is set smaller than a high-frequency power in which said first insulation film contains H_2O with an about of about 1.1 wt % or less.

Claim 3 (Withdrawn): A method as claimed in claim 1, wherein said high-frequency power is set smaller than about 100 W.

Claim 4 (Withdrawn): A method as claimed in claim 1, wherein said high-frequency power is set between about 50 W and about 100 W.

Claim 5 (Withdrawn): A method as claimed in claim 1, wherein said first insulation film has a refractive index of about 1.5.

Claim 6 (Withdrawn): A method as claimed in claim 1, wherein said plasma CVD process is conducted while using SiH_4 and N_2O as source materials, with a proportion of N_2O with respect to SiH_4 set to be about 10 or less.

Claim 7 (Withdrawn): A method as claimed in claim 1, further including a step, after said step of forming said first insulation film and before said step of forming said second insulation film, of annealing said first insulation film.

Claim 8 (Withdrawn): A method as claimed in claim 7, wherein said annealing step is conducted by a rapid heating process.

Claim 9 (Withdrawn): A method as claimed in claim 1, wherein said step of forming said first insulation film and said step of forming said second insulation film are conducted in a common reaction vessel, without a step of taking out said substrate outside said reaction vessel.

Claim 10 (Withdrawn): A method as claimed in claim 1, wherein said step of forming said diffusion region includes a step of forming a silicide on a surface of said diffusion region, and wherein said step of forming said silicide is conducted before said step of forming said first insulation film.

Claim 11 (Withdrawn): A method as claimed in claim 1, further comprising a step, before said step of forming said first insulation layer, of forming a conductor pattern in contact with said diffusion region.

Claim 12 (Withdrawn): A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate;

forming a diffusion region in said substrate adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region; said step of forming said self-aligned opening comprising the steps of:

forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film; forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

removing said first insulation film exposed at a bottom of said contact hole selectively with respect to said diffusion region;

wherein said step of forming said first insulation film is conducted by a CVD process that uses SiH_4 and N_2O as source gases.

Claim 13 (Withdrawn): A method as claimed in claim 12, wherein said CVD process is conducted while setting a ratio of N_2O with respect to SiH_4 to about 5 or less.

Claim 14 (Withdrawn): A method as claimed in claim 12, wherein said CVD process is conducted at a substrate temperature of about 825°C or less.

Claim 15 (Withdrawn): A method as claimed in claim 12, further including a step, after said step of forming said first insulation film and before said step of forming said second insulation film, of annealing said first insulation film.

Claim 16 (Withdrawn): A method as claimed in claim 12, wherein said annealing step is conducted by a rapid heating process.

Claim 17 (Withdrawn): A method as claimed in claim 12, wherein said step of forming said first insulation film and said step of forming said second insulation film are conducted in a common reaction vessel, without a step of taking out said substrate outside said reaction vessel.

Claim 18 (Withdrawn): A method as claimed in claim 12, wherein said step of forming said diffusion region includes a step of forming a silicide on a surface of said diffusion region, and wherein said step of forming said silicide is conducted before said step of forming said first insulation film.

Claim 19 (Withdrawn): A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate;

forming a diffusion region in said substrate adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region;

said step of forming said self-aligned opening comprising the steps of:

forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film;

forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

removing said first insulation film exposed at a bottom of said contact hole selectively with respect to said diffusion region;

wherein said step of forming said first insulation film is conducted by depositing a silicate glass containing P.

Claim 20 (Withdrawn): A method as claimed in claim 19, wherein said silicate glass contains P therein with an amount of about 6 wt % or less.

Claim 21 (Withdrawn): A method as claimed in claim 19, wherein said silicate glass further contains B.

Claim 22 (Withdrawn): A method as claimed in claim 21, wherein said silicate glass contains B with an amount of about 4 wt % or less.

Claim 23 (Withdrawn): A method as claimed in claim 19, further including a step, after said step of forming said first insulation film and before said step of forming said second insulation film, of annealing said first insulation film.

Claim 24 (Withdrawn): A method as claimed in claim 23, wherein said annealing step is conducted by a rapid heating process.

Claim 25 (Withdrawn): A method as claimed in claim 19, wherein said step of forming said first insulation film and said step of forming said second insulation film are conducted in a common reaction vessel, without a step of taking out said substrate outside said reaction vessel.

Claim 26 (Withdrawn): A method as claimed in claim 19, wherein said step of forming said diffusion region includes a step of forming a silicide on a surface of said diffusion region, and

wherein said step of forming said silicide is conducted before said step of forming said first insulation film.

Claim 27 (Withdrawn): A method as claimed in claim 19, further comprising a step, before said step of forming said first insulation layer, of forming a conductor pattern in contact with said diffusion region.

Claim 28 (Previously Presented): A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode;

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region;

wherein said semiconductor device further includes;

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film contains H_2O with an amount smaller than about 2.4 wt%.

Claim 29 (Original): A semiconductor device as claimed in claim 28, wherein said first insulation film contains H_2O with an amount of about 1.1 wt % or less

Claim 30 (Canceled)

Claim 31 (Previously Presented): A semiconductor device as claimed in claim 28, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends along a surface of said side wall oxide film.

Claim 32 (Canceled)

Claim 33 (Previously Presented): A semiconductor device as claimed in claim 28, further comprising another silicide region formed selectively on a surface of said gate electrode.

Claim 34 (Previously Presented): A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on side wall of said gate electrode;

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region,

wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of PSG containing P with an amount of about 6 wt% or less.

Claim 35 (Previously Presented): A semiconductor device as claimed in claim 34, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends along a surface of said side wall oxide film.

Claim 36 (Canceled)

Claim 37 (Previously Presented): A semiconductor device as claimed in claim 34, further comprising another silicide region formed selectively on a surface of said gate electrode.

Claim 38 (Previously Presented): A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode;

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region,

wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of BPSG containing B with an amount of about 4 wt% or less.

Claim 39 (Previously Presented): A semiconductor device as claimed in claim 38, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends along a surface of said side wall oxide film.

Claim 40 (Canceled)

Claim 41 (Previously Presented): A semiconductor device as claimed in claim 38, further comprising another silicide region formed selectively on a surface of said electrode

Claim 42 (Withdrawn): A method of fabricating a semiconductor device, comprising the steps of:

(A) forming a refractory metal layer on a diffusion region in a semiconductor substrate;

(B) forming a self-aligned silicide layer on said refractory metal layer by applying a heat-treatment process;

(C) forming an insulation film on a surface of said silicide layer by conducting a plasma CVD process while using a source gas containing SiH4 and N_2O with a ratio of N_2O with respect to SiH4 equal to or less than 5;

(D) forming a nitride film, after said step (C), on said insulation film in contact with said insulation film, without exposing a surface of said insulation film to the air;

(E) forming an interlayer insulation film so as to cover said nitride film; and

(F) forming a window exposing said silicide layer, by applying a dry etching process consecutively to said interlayer insulation film, said nitride film, and said insulation film.

Claim 43 (New): A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode;

a self-aligned contact hole defined by said sidewall oxide film and exposing said diffusion region;

a silicide region formed selectively on a surface of said diffusion region;

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film; and

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole,

wherein said first insulation film is formed by a plasma CVD process with a plasma power of 100W or less and contains H_2O with an amount smaller than about 1.1 wt%, and said first insulation film has a refractive index of 1.5 or less.